SNEHA ARUN LELE

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PROFILE

Electronics/Optical design and test engineer with a doctorate, four years of industry experience and more than five years of analog/digital circuit design, analysis, optimization and signal processing experience. Hard-working, result-oriented and adaptable, with a keen interest in design of integrated microsystems.

PROFESSIONAL EXPERIENCE

New Product Introduction Test Engineer Feb 2015 - Present
ADVA Optical Networking *Greater Atlanta Area, U.S.A.*

- Design, development and deployment of end to end manufacturing test solutions.
- Architect test concepts and design hardware and software interfaces for testing optical networking equipment.
- Involved in board level and component level functional testing of WDM telecom devices and optical EDFAs using NI TestStand and LabVIEW.

Analog Design Engineer Oct 2013 - Oct 2014
Advanced Micro Devices, Inc. (AMD) *Markham ON, Canada*

- Part of the team involved in design of the DisplayPort AUX/I2C interface for TSMC28, GF28, GF20 and GF14 technologies.
- Involved in development and execution of pre-silicon verification test plans to validate IP/chip functions.
- Involved in post-layout simulation, characterization, debug, timing, ESD and EMIR analysis of analog circuits for IO interface and custom macros.

Teaching Assistant Sept 2009 - April 2013
The University of Western Ontario *London ON, Canada*

- Tutored third year engineering students in learning Cadence to perform schematic and layout simulations, increasing students' knowledge in design systems and analytical skills.
- Instructed first year engineering students with no programming background, to use VisualC++.

Executive Engineer July 2006 - July 2008
Siemens Ltd. (Transportation Systems) *Mumbai, India*

- Involved in the design improvisation of '25kVA underslung type coach converter' typically used in air conditioning systems in Indian Railway coaches.
- Successfully integrated the 'earth fault bypass' module in the Siemens made system software SIBMON of 180kVA converter.
- Part of the team developing the 500kVA converter for power car of super fast trains of Indian Railways, and its corresponding control panel, for the air conditioning and lighting loads in each coach.

TECHNICAL STRENGTHS

Languages	C, C++, GNU Octave, LaTeX, VHDL, Perl, HTML
Software	Matlab, LabView, NI TestStand, ISE Design, PSCAD, COMSOL, SolidWorks
EDA & Simulation tools	Cadence, Totem (MMX, Pathfinder), Eagle PCB, SPICE, KiCAD
Systems	Windows (98, 2000, XP, Vista, 7), GNU/Linux, Mac OS

EDUCATION

Doctorate of Philosophy (Ph.D.) Sept 2009 - Sept 2013
(Completed on Sept 17, 2013)
Masters of Engineering Science (M.E.Sc.) Sept 2008 - August 2009
(Transfered to doctoral program)
Department of Electrical and Computer Engineering (ECE)
The University of Western Ontario, London ON, Canada
Bachelor of Engineering (B.E.) Sept 2002 - June 2006
Department of Electronics, VESIT,
Mumbai University, Mumbai, India

PROJECTS

Integrated Sensing Devices for High-voltage Power System Lines Sept 2009 - Sept 2013

Research, in association with GE Multilin, based on integration of control circuits for power relays. The objective was to develop a microsystem methodology to detect voltage and current disturbances in high-voltage power distribution lines. The system employed a piezoelectric transformer and Hall-effect sensor with an integrated signal processing unit designed using Cadence Spectre, COMSOL, PSCAD/EMTDC, Matlab and active/passive circuits.

3D piezoelectric transformer and thermocouple principle modeling Oct - Dec 2010

Modeling of a 3D piezoelectric transformer in COMSOL and its eigen, frequency and time domain analysis using real-time voltage signals. To understand the phenomenon of temperature measurement and control in integration of circuits, thermocouple principle was also simulated.

Simple brain-machine interface circuit using FPGAs Feb 2010 - April 2010

Brain-machine prototype extended to design an FPGA-based BMI development platform using Xilinx ISE Design Suite 11 for Virtex5 family, to generate simple on-off commands to control a robotic manipulator based on decoded brain signals, using VHDL.

Steady-state Visually Evoked EEG Signal Processing with Tuneable Continuous-time Bandpass Sigma-Delta Modulators Dec 2008 - March 2009

Signal Processing unit designed for $0.18\mu m$ CMOS process for application in a non-invasive brain-machine interface system, which allows the simple control of a switch.

Behavioral modeling of mixed-signal systems Sept - Dec 2008

Schematic, layout, DRC, LVS, parasitic extraction, and analysis of noise margin, propagation delay, power dissipation of basic gates in Cadence ($0.18\mu m$ CMOS technology). Behavioral modeling of amplifier circuits, filter circuits, closed loop systems, adaptive equaliser, PLL and Sigma-Delta modulator using Cadence Verilog-A ModelWriter tool.

Wireless collection of train maintenance data June - July 2006
Delhi Metro Rail Corporation (DMRC)

This project involved reliable wireless transmission of data from metro trains to transceivers placed up to 150 meters away, that involved replacing the existing wired RS232 link using two solutions, ZigBee transceivers and WiFi routers.